

REMARKS

The Final Office Action dated January 26, 2005, has been received and reviewed.

Claims 1-39 and 41-67 are currently pending in the above-referenced application. Of these, the Office has withdrawn claims 14-16, 27-30, 34-36, 41, and 45-67 from consideration. Claims 1-13, 17-26, 31-33, 37-39, and 42-44, which have been considered, stand rejected.

Reconsideration of the above-referenced application is respectfully requested.

Supplemental Information Disclosure Statements

Please note that Supplemental Information Disclosure Statements were filed in the above-referenced application on November 2, 2004, and January 26, 2005, but that the undersigned attorney has not yet received any indication that the references cited in these Supplemental Information Disclosure Statements have been considered in the above-referenced application. It is respectfully requested that the references cited in the Supplemental Information Disclosure Statements of November 2, 2004, and January 26, 2005, be considered and made of record in the above-referenced application and that initialed copies of the Forms PTO/SB/08A that accompanied these Supplemental Information Disclosure Statements be returned to the undersigned attorney as evidence of such consideration.

If any of the documents or any portion thereof are not available to the Office, the undersigned attorney would be happy to supply a copy thereof.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 19-26, 33, and 42-44 stand rejected under 35 U.S.C. § 112, second paragraph, for reciting subject matter that would purportedly not be definite to one of ordinary skill in the art.

In particular, the Office has objected to independent claim 19 on the basis that it is not clear whether “the intermediate conductive element . . . or the nonconfluent spacer layer” recited in independent claim 19 protrudes from the surface of a first semiconductor device “the same distance the active surface of the first semiconductor device is to be spaced from a back side of a second semiconductor device . . .” Final Office Action, page 2.

The use of commas in independent claim 19 clearly indicates that it is the nonconfluent spacer layer, rather than the intermediate conductive element, that protrudes from the active

surface substantially a same distance the active surface of the first semiconductor device is to be spaced apart from a back side of a second semiconductor device.

This fact is reiterated by the recitation in independent claim 19 that the semiconductor device assembly need not include an intermediate conductive element.

The Office has also asked for a reference to the drawings to support the language recited in independent claim 19. The Office is reminded that it has not rejected independent claim 19 under the first paragraph of 35 U.S.C. § 112. Thus, no reference to the drawings is necessary to explain why one of ordinary skill in the art would understand that it is the dielectric spacer layer, not the at least one intermediate conductive element, that protrudes from the surface of a die substantially a predetermined distance.

Claims 20-26, 33, and 42-44 have been rejected merely for depending directly or indirectly from independent claim 19.

In view of the foregoing, withdrawal of the 35 U.S.C. § 112, second paragraph rejections of claims 19-26, 33, and 42-44 is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-13, 17-26, 31-33, 37-39, and 42-44 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.
In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Foster

Claims 1-10, 17, 19-26, 33, and 42-44 are under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the subject matter taught in U.S. Patent 6,552,416 to Foster (hereinafter “Foster”).

Foster teaches a variety of multichip modules that include tape 32, die attach paste 33, and inner-lead traces 20 between stacked dies 30 and 31. *See, e.g.*, FIG. 8; col. 4, lines 50-57; col. 5, lines 16-23. In particular, the multichip module shown in FIG. 8 of Foster includes a lower die 31 with centrally located bond pads, a first layer of die attach paste 33 on regions of the active surface of the lower die 31, which secures inner-lead traces 20 to the active surface of the lower die 31, tape 32 over the inner-lead traces 20, and a second layer of die attach paste 33 securing the tape 32 to the back side of another, upper semiconductor die 30. *Id.*

The combined thicknesses of the first layer of die attach paste 33, the inner-lead traces 20, the tape 32, and the second layer of die attach paste 33 may be substantially the same as the distance the lower die 31 and an upper die 30 are to be spaced apart from one another. Nonetheless, from col. 4, lines 63-67, of Foster, it is clear that bond wires 35 must be secured to the bond pads of the lower die 31 *before* the second layer of die attach paste 33 is placed over the inner-lead traces 20. Thus, these layers do not have their final, combined height, *i.e.*, the height that will space the upper die 30 substantially a predetermined distance from a surface of the lower die 31, until *after* bond wires 35 are in place.

Independent claim 1 recites a semiconductor device that includes a semiconductor die and a dielectric spacer layer that protrudes substantially a predetermined distance from a surface of a semiconductor die before an intermediate conductive element is secured to a bond pad of the semiconductor die. The predetermined distance accommodates a height of at least one intermediate conductive element between the semiconductor die and an adjacent semiconductor die.

While the recitation that the dielectric spacer layer protrudes from a surface of a semiconductor die substantially the predetermined distance *before* an intermediate conductive element is secured to a bond pad of the semiconductor die may be considered functional language, it is important “for what it reasonably conveys to a person of ordinary skill in the pertinent art in the contact of which it is used” (M.P.E.P. § 2173.05(g)) – an understanding that

the claimed semiconductor device need not include an intermediate conductive element (bond wire or otherwise), as well as an understanding that the dielectric spacer layer already has its full height before an intermediate conductive element (bond wire or otherwise) is secured to a bond pad of the semiconductor die from which the dielectric spacer layer protrudes. Therefore, the Office cannot ignore language regarding the distance the dielectric spacer protrudes from a surface of a semiconductor die *before* at least one intermediate conductive element is secured to a bond pad of the semiconductor die.

That being stated, a *prima facie* case of obviousness has not been established against independent claim 1 because Foster does not teach or suggest each and every element of independent claim 1. In particular, Foster does not teach or suggest that the first layer of die attach paste 33, the inner-lead traces 20, the tape 32, and the second layer of die attach paste 33, the combined thicknesses of all of which are necessary to accommodate the height of an intermediate conductive element (*e.g.*, bond wire 35), are all positioned over lower die 31 before an intermediate conductive element (*e.g.*, bond wire 35) is secured to a bond pad of the lower die 31. Rather, the teachings of Foster are limited to adding the second layer of die attach paste 33 *after* bond wires 35 are secured to the bond pads of the lower die 31. Col. 4, lines 63-67.

Therefore, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 1 is allowable over that disclosed in Foster.

Each of claims 2-10 and 17 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 6 is additionally allowable because Foster does not teach or suggest that the predetermined distance that the multi-layered spacing elements thereof protrude from the surface of the lower semiconductor die 31 is the same as or less than the distance the bond wires 35 protrude above the surface of the lower semiconductor die 31. Rather, the teachings of Foster are limited to a series of layers that protrude from the surface of a lower die 31 a distance that exceeds the height that a bond wire 35 protrudes from the surface of the lower die 31.

Claim 9 is further allowable since Foster lacks any teaching or suggestion that the multi-layered spacing elements thereof may include randomly arranged features.

Independent claim 19 is directed to a semiconductor device assembly that includes a first semiconductor device and a nonconfluent spacer layer. The nonconfluent spacer layer includes dielectric material secured to the active surface of the first semiconductor device. The nonconfluent spacer layer protrudes from the active surface substantially a same distance that the active surface of the first semiconductor device is to be spaced apart from a back side of a second semiconductor device, even before an intermediate conductive element is secured to any of the bond pads of the first semiconductor device.

Again, the recitation that the nonconfluent spacer layer protrude a particular distance from the active surface of a first semiconductor device before an intermediate conductive element is secured to a bond pad of the first semiconductor device conveys to one of ordinary skill in the art that the nonconfluent spacer layer has been imparted with its full height, or thickness, before an intermediate conductive element is secured to a bond pad of the first semiconductor device.

Foster does not teach or suggest that the first layer of die attach paste 33, the inner-lead traces 20, the tape 32, and the second layer of die attach paste 33 are all positioned over lower die 31 *before* an intermediate conductive element (*e.g.*, bond wire 35) is secured to a bond pad of the lower die 31. Instead, Foster teaches that the second layer of die attach paste 33 is not added until *after* bond wires 35 are secured to the bond pads of the lower die 31. Col. 4, lines 63-67.

As such, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 19 is directed to subject matter which is allowable over that described in Foster.

Claims 20-26, 33, and 42-44 are each allowable, among other reasons, for depending either directly or indirectly from claim 19, which is allowable.

Claim 26 is additionally allowable because Foster does not teach or suggest that the predetermined distance that the multi-layered spacing elements thereof protrudes from the surface of the lower semiconductor die 31 is the same as or less than the distance the bond wires 35 protrude above the surface of the lower semiconductor die 31.

Shim

Claims 1-10, 13, 17, 19-26, 32, 33, 37-39 and 42-44 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 6,531,784 to Shim et al. (hereinafter “Shim”).

Shim teaches elongated spacer strips 50A, 50B. FIGs. 4-6; col. 4, lines 33-38. The spacer strips 50A, 50B of Shim are formed from insulative material. Col. 4, lines 50-53. Apparently, the spacer strips 50A, 50B of Shim are preformed, as the teachings of Shim are limited to attachment or mounting (*e.g.*, with adhesive) thereof to a top surface of a semiconductor die 14. Col. 4, lines 56-60; col. 5, line 19; col. 5, lines 32-37; col. 5, lines 62-66.

Spacer strips 50A, 50B do not protrude from the top surface of semiconductor die 14 substantially the same distance that semiconductor die 14 is to be spaced apart from another semiconductor die 16. Rather, as shown in FIGS. 3, 7, 8, and 9 of Shim, once bond wires are secured to the bond pads of semiconductor die 14 and to corresponding terminals of a substrate upon which semiconductor die 12 is positioned, an additional adhesive 44 (*see also*, col. 5, lines 10-14) or spacer strip 50C (*see also*, col. 6, lines 6-19) is required to space the second semiconductor die 16 the predetermined distance apart from the active surface of the first semiconductor die 14.

Shim includes no teaching or suggestion of a semiconductor device that includes a dielectric spacer layer that protrudes from a surface of a semiconductor die a predetermined distance that the semiconductor die is to be spaced apart from another semiconductor die *before* at least one intermediate conductive element is secured to a bond pad of the semiconductor die, as is required by independent claim 1. Instead, the teachings of Shim are limited to spacer strips 50A, 50B that protrude from the surface of a semiconductor die 14 only a portion of the distance the semiconductor die 14 is to be spaced apart from another semiconductor die 16.

Therefore, Shim does not support a *prima facie* case of obviousness against independent claim 1, as would be required to maintain the 35 U.S.C. § 103(a) rejection of independent claim 1.

Claims 2-10, 13, and 17 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 6 is additionally allowable because Shim does not teach or suggest that the predetermined distance that the spacer strips 50A, 50B thereof protrudes from the surface of the lower semiconductor die 14 is the same as or less than the distance the bond wires or other intermediate conductive elements protrude above the surface of the lower semiconductor die 14.

Claim 9 is further allowable since Shim lacks any teaching or suggestion that the spacer strips 50A, 50B thereof may include randomly arranged features.

With respect to the subject matter recited in independent claim 19, Shim lacks any teaching or suggestion of a semiconductor device assembly that includes a first semiconductor device with a nonconfluent spacer layer protruding from an active surface thereof substantially a predetermined distance the active surface is to be spaced apart from a back side of the second semiconductor device *before* an intermediate conductive element, such as a bond wire, is secured to any of the bond pads at the active surface of the first semiconductor device. Rather, the spacers of Shim are not provided with their full heights, which are equal to the distances that semiconductor dice 14 and 16 are spaced apart from one another, until after intermediate conductive elements are secured to the bond pads of the lower semiconductor die 14.

Therefore, under 35 U.S.C. § 103(a), independent claim 19 is directed to subject matter which is allowable over the subject matter described in Shim.

Each of claims 20-26, 32, 33, 37-39, and 42-44 is allowable, among other reasons, for depending either directly or indirectly from claim 19, which is allowable.

Claim 26 is additionally allowable because Shim neither teaches nor suggests that the predetermined distance that the spacer strips 50A, 50B thereof protrudes from the surface of the lower semiconductor die 14 is the same as or less than the distance that bond wires or other intermediate conductive elements protrude above the surface of the lower semiconductor die 14.

Shim in View of Smith

Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is assertedly unpatentable over the teachings of Shim, in view of teachings from U.S. Patent 6,049,370 to Smith, Jr., et al. (hereinafter “Smith”).

Claims 11 and 12 are allowable, among other reasons, for depending from claim 1, which is allowable.

Shim in View of Blanton

Claims 18 and 31 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the subject matter taught in Shim, in view of the teachings of U.S. Patent 5,220,200 to Blanton (hereinafter “Blanton”).

Claim 18 is allowable, among other reasons, for depending from claim 1, which is allowable.

Claim 31 is allowable, among other reasons, for depending from claim 19, which is allowable.

Foster in View of Mueller

Claims 11, 13 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,552,416 to Foster in view of U.S. Patent 6,316,786 to Mueller et al. Applicant respectfully traverse this rejection, as hereinafter set forth.

Claims 11 and 13 are both allowable, among other reasons, for depending directly from claim 1, which is allowable.

Claim 32 is allowable, among other reasons, for depending directly from claim 19, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-13, 17-26, 31-33, 37-39, and 42-44 be withdrawn.

ELECTION OF SPECIES REQUIREMENT

Independent claim 1 remains generic to all of the species of invention that were identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 14-16, 27-30, 34-36, 41, and 45-67, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

CONCLUSION

It is respectfully submitted that each of claims 1-39 and 41-67 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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